Claims

What is claimed is:

1. A method for manufacturing a block alterable memory cell, such method comprises the following steps:

depositing a screen oxide over a substrate layer;

depositing a mask implant layer over the screen oxide layer;

implanting memory cells in the portion of the substrate layer not covered by the mask implant layer;

etching a screen oxide and an initial gate oxide from memory cells;

depositing tunnel window mask;

etching a tunnel oxide layer;

depositing control poly layer; and

implanting source and drain regions.

2. The method for manufacturing a block alterable memory cell of claim 1, wherein the step of deposing a control poly layer further comprising:

depositing a first oxide layer;

depositing an inter poly layer;

depositing a second oxide layer.

3. The method for manufacturing a block alterable memory cell of claim 1, wherein said tunnel oxide layer having a thickness of 50-70 angstroms.

4. The method for manufacturing a block alterable memory cell of claim 1, wherein said screen oxide layer having a thickness of 200-350 angstroms.

5. A block alterable memory cell, comprising:

a substrate layer having a source implant region, an active region, a floating gate transistor region, and a drain implant region;

a tunnel oxide layer overlying said substrate layer;

a first layer overlying said tunnel oxide layer;

an inter poly layer overlying over said first oxide; and

a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region.

6. The block alterable memory cell of claim 5, wherein the substrate layer is a p type doping substrate.

7. The block alterable memory cell of claim 5, wherein the source implant region, said drain implant region, and said floating gate transistor region are n type implants.

8. The block alterable memory cell of claim 5, wherein the first layer and said second layer are oxide layers.

9. The block alterable memory cell of claim 5, wherein the inter poly layer is a nitride layer.

10. The block alterable memory cell of claim 5, wherein the substrate layer further comprises a thin surface layer.

11. A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns;

an input/output port in communication with said memory array;

a controller coupled to said input/output port and said memory array;

wherein said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell further comprising:

a substrate layer having a source implant region, an active region, a floating gate transistor region, and a drain implant region;

a tunnel oxide layer overlying said substrate layer;

a first layer overlying said tunnel oxide layer;

an inter poly layer overlying over said first oxide; and

a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region.